## DIGITAL SYSTEM DESIGN

**(CE-304L)**

# FINAL LAB EXAM

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| **Date** | 23,24,25,26 January 2023 |  |
| **Time** | 02 hours |
| **Marks** | 20 |
| **Instructors** | Engr. Maqsood Jan Mohammad  Engr. Muhammad Irfan ul haq Malik |

**INSTRUCTIONS:**

1. Read the questions carefully before answering.
2. Answers should be on the same paper.
3. Attempt all parts. Extra marks for attempting FSM choice
4. Attempting a question will earn you credit, leaving it blank will not. Choose wisely.

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| |  |  | | --- | --- | | **Name:** |  | | **Roll Number:** |  | | **Marks Obtained:** | **/ 20** | | | | |
| **Question 01** | **[CLO 1 – PLO 5 – C3]** | **(20 Marks)** | |
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| 1. Draw the truth table of the above functions & . | | | (04) |
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| 1. Draw the schematic of functions & . | | | (03) |
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| 1. Write a design module (Verilog) performing above functions ( & ) using Data Flow modeling in ISE. | | | (05) |
| **Verilog Module:**   * + - * 1. `timescale 1ns / 1ps         2. //////////////////////////////////////////////////////////////////////////////////         3. // Company:         4. // Engineer:         5. //         6. // Create Date: 11:46:41 01/23/2023         7. // Design Name:         8. // Module Name: combineLogic         9. // Project Name:         10. // Target Devices:         11. // Tool versions:         12. // Description:         13. //         14. // Dependencies:         15. //         16. // Revision:         17. // Revision 0.01 - File Created         18. // Additional Comments:         19. //         20. //////////////////////////////////////////////////////////////////////////////////         21. module combineLogic(         22. input a,         23. input b,         24. input c,         25. output f1,         26. output f2         27. );         28. wire b0, a0, c0, ab0c, a0bc, abc0, a0bc0;         29. not(a0, a);         30. not(b0, b);         31. not(c0, c);         32. and(ab0c, a, b0, c);         33. and(a0bc, a0, b, c);         34. and(abc0, a, b, c0);         35. and(a0bc0, a0, b, c0);         36. or(f1, ab0c, a0bc, abc0, a0bc0);         37. and(f2, a0+b0+c, a+b+c);   endmodule   1. Draw the truth table of the above functions & . | | |  |
| 1. Write a test fixture (Verilog) for the design module & simulate it in ISE. | | | (05) |
| **TEXTFIXTURE**   * + - * 1. `timescale 1ns / 1ps         2. ////////////////////////////////////////////////////////////////////////////////         3. // Company:         4. // Engineer:         5. //         6. // Create Date: 11:56:37 01/23/2023         7. // Design Name: combineLogic         8. // Module Name: F:/ISE PROJECTS/labTask/testBench.v         9. // Project Name: labTask         10. // Target Device:         11. // Tool versions:         12. // Description:         13. //         14. // Verilog Test Fixture created by ISE for module: combineLogic         15. //         16. // Dependencies:         17. //         18. // Revision:         19. // Revision 0.01 - File Created         20. // Additional Comments:         21. //         22. ////////////////////////////////////////////////////////////////////////////////         23. module testBench;         24. // Inputs         25. reg a;         26. reg b;         27. reg c;         28. // Outputs         29. wire f1;         30. wire f2;         31. // Instantiate the Unit Under Test (UUT)         32. combineLogic uut (         33. .a(a),         34. .b(b),         35. .c(c),         36. .f1(f1),         37. .f2(f2)         38. );         39. initial begin         40. // Initialize Inputs         41. a = 0;         42. b = 0;         43. c = 0;         44. #100;         45. a = 1;         46. b = 0;         47. c = 0;         48. #100;         49. a = 0;         50. b = 1;         51. c = 0;         52. #100;         53. a = 0;         54. b = 0;         55. c = 1;         56. #100;         57. a = 1;         58. b = 1;         59. c = 0;         60. #100;         61. a = 1;         62. b = 1;         63. c = 1;         64. #100;         65. a = 0;         66. b = 0;         67. c = 0;         68. #100;         70. end         72. endmodule   **WAVE Form:**  \ | | |  |
| 1. Viva | | | (03) |